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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,397	04/11/2006	Takefumi Nishimuta	5000-5295	2526

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EXAMINER	
PATTON, PAUL E	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
10/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/560,397	NISHIMUTA ET AL.	
	Examiner	Art Unit	
	Paul E. Patton	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *7&8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/26/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Acknowledgement is made of Amendment filed July 26, 2007

2. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1- 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuru (JP 09-323292) Mitsuru, in view of Hieda (JP 2001-224740) Hieda and in view of Ohmi (USPAT 6975018 B2) Ohmi and further in view of Shimazaki et al. (US 2001/0043085 A1) Shimazaki.

5. As to claims 1 and 6, Mitsuru discloses and shows (Fig 2) a switch formed by connecting in parallel a p-channel MIS field-effect transistor (51) with an n-channel MIS field-effect transistor (50) and including a capacitor (4).

6. Mitsuru does not disclose transistors in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in a plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of the top surface and the side surface of the projecting portion at a temperature at

or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; wherein gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

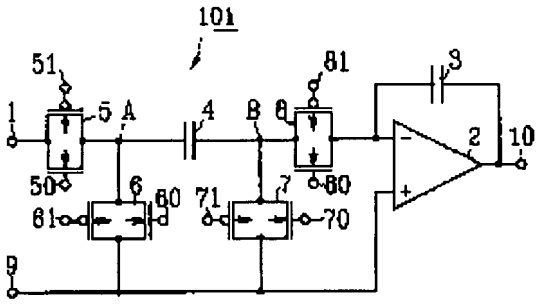

Fig 2

7. Hieda discloses and shows (Fig 1) a MIS Field-effect transistors, both p-channel and n-channel (Fig 48) in which a projecting portion (17) is formed by a silicon substrate (10) having a first crystal surface (13) as a primary surface and a second crystal surface (17) as a side surface, a gate insulating film (18) is formed on at least part of the top surface and the side surface of the projecting portion, a gate (16) is formed on the gate insulating film, and a drain and a source (22) are formed on both sides enclosing the gate insulating film of the projecting portion.

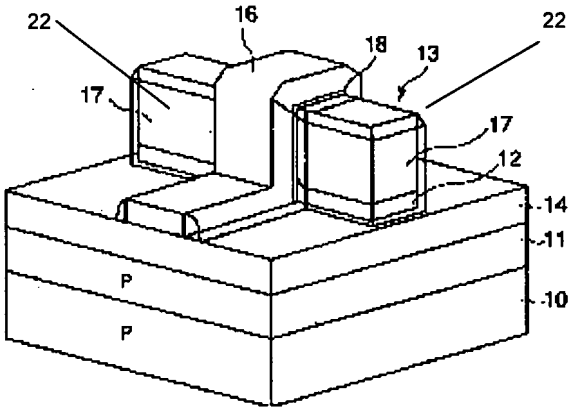

Fig 1

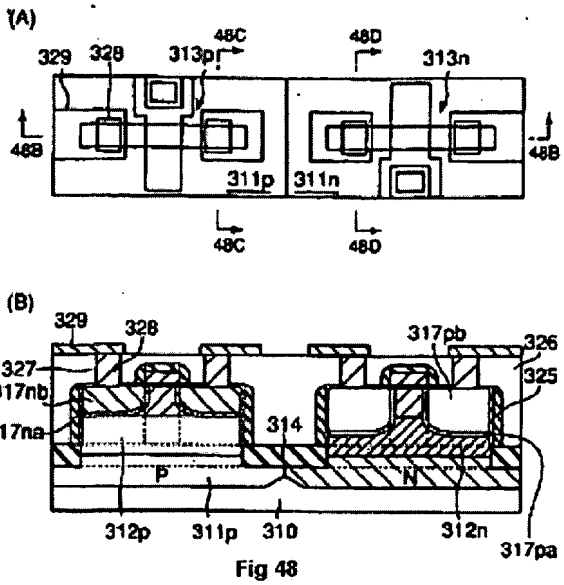

Fig 4B

8. Heida is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use a MIS Field-effect transistors, both p-channel and n-channel in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, a gate insulating film is formed on at least part of the top surface and the side surface of the projecting portion, a gate is formed on the gate insulating film, and a drain and a

source are formed on both sides enclosing the gate insulating film of the projecting portion.

9. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mitsuru by using a MIS Field-effect transistors, both p-channel and n-channel in which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, a gate insulating film is formed on at least part of the top surface and the side surface of the projecting portion, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion for advantages such as suppressing short channel effects according to the teachings of Heida. (Paragraph [0013])

10. Mitsuru as modified by Hieda does not disclose that terminated hydrogen on the silicon surface is removed in a plasma atmosphere on an inert gas, nor does he state that the gate insulating film is formed at a temperature at or lower than about 550°C in the plasma atmosphere.

11. Ohmi discloses that terminated hydrogen on the silicon surface is removed in a plasma atmosphere or an inert gas (Column 3, lines 50-53), and states that the gate insulating film is formed at a temperature at or lower than about 550°C in the plasma atmosphere (Column 4, lines 26-32)

12. Ohmi is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to use plasma and inert gas to remove terminated hydrogen and to form a gate insulating film at temperatures at or lower than about 550°C.

13. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mitsuru and Hieda by using plasma and inert gas to remove terminated hydrogen and to form a gate insulating film at temperatures at or lower than about 550°C to obtain advantages such as maintaining uniformity of film formation across large substrates and reduced leakage current according to the teachings of Ohmi (Column 1,lines 42-48 and Column 2, lines 1-10).

14. Mitsuru as modified by Heida and Ohmi does not disclose that the gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

15. Shimazaki discloses that the gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor. (Paragraph [0128]).

16. Shimazaki is evidence that a person of ordinary skill in the art would find a reason, suggestion or motivation to design the gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

17. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Mitsuru, Hieda and Ohmi by design the gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor for advantages such as developing high speed logic circuits according to the teachings of Ohmi. (Paragraph [0128]).

18. As to claim 2, Mitsuru as modified by Hieda, Ohmi and Shimazaki discloses and shows (Heida, Fig 1) that a channel (22) is formed on a first crystal surface of a top surface (13) and a second crystal surface (17) of the projecting portion and the channel width of the MIS field-effect transistor is a total of a channel width of the top surface and a channel width of the side surface (Hieda, paragraph [0016]).

19. As to claim 3, Mitsuru as modified by Hieda, Ohmi and Shimazaki discloses and shows (Fig 1 and 48) the projecting portion has a top surface comprising a silicon surface (100) (Paragraph [0036]), and the source (S) and drain (D) are formed on the projecting portion enclosing the gate and in left and right area of the projecting portion of the silicon substrate (Fig 48).

20. Hieda does not explicitly disclose that the side surface of the projecting portion has a crystal orientation of (110). Given the well-known nature of crystalline silicon the orientation of the side surface as (110) would have at least been obvious.

21. As to claim 4, Mitsuru shows (Mitsuru, Fig 2) a switched capacitor circuit comprising a switch formed by connecting in parallel a p-channel MIS field-effect transistor and n-channel field-effect transistor.

22. Mitsuru as modified by Heida, Ohmi and Shimazaki discloses that the gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor. (Paragraph [0128]).

23. As to claim 5, Mitsuru as modified by Heida, Ohmi and Shimazaki shows (Mitsuru, Fig 2) the switched capacitor circuit comprises: first p-channel and n-channel MIS field effect transistors (Mitsuru, 50,51) which receive a signal at an input terminal (1), and are connected in parallel to each other; second p-channel and n-channel MIS transistors (Mitsuru, 60,61) which are connected to each other, whose input terminals are connected to output terminals of the first p-channel and n- channel MIS field-effect transistor, and whose output terminals are grounded; a capacitor (Mitsuru, 4) one terminal of which is connected to an output terminal of the first p-channel and n-channel MIS field-effect transistors; third p-channel and n-channel MIS field-effect transistors (Mitsuru, 70,71) which are connected in parallel to each other, whose input terminal is connected to another terminal of the capacitor, and whose output terminal is grounded; and fourth p-channel and n-channel MIS field-effect transistors (Mitsuru, 80,81) which are connected in parallel to each other and whose input terminal is connected to another terminal of the capacitor.

24. It is further noted that while all the claims have been shown to be known in the art, with respect to claims 1 and 6 with the exception of the circuit elements disclosed by Mitsuru, and all the limitations of claims 2, 3 and 4 are considered as a product by process claims. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even thought the prior product was made by a different process." In re Thorpe, 777F, 2d 659, 698, 227 USPQ 964, 966 (Fed. Cir. 1985); see also MPEP 2113.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Patton whose telephone number is 571-272-9762. The examiner can normally be reached on 7:00 - 5:30 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul E Patton
Examiner
Art Unit 2822

PEP

Zandra V. Smith
Supervisory Patent Examiner
10 oct - 2007